S/N 09/928,224 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Nick A. Youker et al.	Examiner: Unknown	
Serial No.:	09/928,224	Group Art Unit: 2814	
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Title:	INTEGRATED EMI SHIELD UTILIZING A HYBRID EDGE		

SUPPLEMENTAL PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the above-identified patent application as follows:

IN THE CLAIMS

Please cancel claims 5 - 9 without prejudice or disclaimer and add the following claims:

13.(New) A method for providing electromagnetic interference edge shielding to an integrated circuit chip carrier, the chip carrier including top and bottom surfaces and an edge, and at least one internal electric ground layer, the method comprising:

forming at least a portion of the internal ground layer along at least a portion of the chip carrier edge;

applying an electrically conductive layer to at least a portion of the chip carrier edge, the conductive layer being applied over the exposed portion of the ground layer and in electrical contact with said ground layer; and

forming at least one cavity within the top surface of the chip carrier, where the at least one cavity configured to hold one or more integrated circuit chips therein.

14.(New) The method as recited in claim 13, further comprising one or more steps within the at least one cavity.

15.(New) The method as recited in claim 14, further comprising forming bonding pads on the one or more steps within the at least one cavity.

16.(New) The method as recited in claim 13, further comprising applying the electrically conductive layer to the entire edge of the integrated circuit chip carrier.

17. (New) The method as recited in claim 13, further comprising mounting circuitry within the at least one cavity.

18.(New) A method for providing electromagnetic interference edge shielding to an integrated circuit chip carrier, the chip carrier including top and bottom surfaces and an edge, and at least one internal ground layer, the method comprising:

exposing at least a portion of the internal ground layer along at least a portion of the chip carrier edge;

applying an electrically conductive layer to at least a portion of the chip carrier edge, the conductive layer being applied over the exposed portion of the internal ground layer and in electrical contact with said internal ground layer; and

forming at least one cavity within the top surface of the chip carrier, where the at least one cavity configured to hold one or more integrated circuit chips therein;

forming two or more steps within the at least one cavity; and

forming bonding pads on each of the steps.

19. (New) The method as recited in claim 18, further comprising applying the electrically conductive layer to the entire edge of the integrated circuit chip carrier.

20. (New) The method as recited in claim 18, further comprising forming conduction paths within the integrated circuit chip carrier, where the conduction paths are configured to allow electrical communication with an external device.

21. (New) The method as recited in claim 18, further comprising introducing metal through capillary action, including filling voids and providing a solid conduction path.

22. (New) The method as recited in claim 18, further comprising coating the bonding pads with a noble metal layer.

23.(New) The method as recited in claim 18, wherein applying the electrically conductive layer includes applying metalized paste to the edge and in electrical contact with the internal ground layer.

24.(New) The method as recited in claim 23, further comprising sintering the chip carrier after the paste is applied to the edge.

25. (New) A method for providing electromagnetic interference edge shielding to an integrated circuit chip carrier, the chip carrier including top and bottom surfaces and an edge, the method comprising:

forming an internal ground layer within the integrated circuit chip carrier;

exposing at least a portion of the internal ground layer along at least a portion of the chip carrier edge;

forming an electrically conductive layer on at least a portion of the chip carrier edge, the conductive layer being applied over the exposed portion of the ground layer and in electrical contact with said ground layer; and

forming at least two cavities within the top surface of the chip carrier, where the cavities each contain circuitry therein;

forming two or more steps within at least one cavity; and

forming bonding pads on each of the steps.

26. (New) The method as recited in claim 25, further comprising forming the electrically conductive layer on the entire edge of the integrated circuit chip carrier.

27. (New) The method as recited in claim 25, wherein forming the electrically conductive layer includes printing the electrically conductive layer on the chip carrier edge.

28. (New) The method as recited in claim 25, wherein forming the electrically conductive layer includes plating the electrically conductive layer on the chip carrier edge.

29. (New) The method as recited in claim 25, wherein forming the electrically conductive layer includes sawing the chip carrier and exposing a hybrid horizontal ground plane.

30. (New) A method for providing electromagnetic interference edge shielding, the method comprising:

stacking-up a plurality of ceramic sheets;

applying a circuit ground layer to at least one ceramic sheet;

applying heat and pressure to the stack-up including sintering the ceramic sheets into a monolithic structure metalizing the circuit ground layer;

exposing at least a portion of the circuit ground layer on an edge surface of the plurality of ceramic sheets;

applying a second electrically conductive layer to at least a portion of the edge surface and in electrical contact with the circuit ground layer;

sintering the ceramic sheets and second electrically conductive layer to metalize the second conductive layer and to create a consolidated chip carrier;

forming at least one cavity within a first surface of the chip carrier; and

mounting circuitry within the at least one cavity.

31. (New) The method as recited in claim 30, wherein exposing the circuit ground layer includes sawing the through portions of the circuit ground layer.

32. (New) The method as recited in claim 30, further comprising forming multiple cavities within the first surface of the chip carrier.

33. (New) The method as recited in claim 32, further comprising forming two or more steps within at least one of the cavities.